CLAIMS

1. An equalizer arranged and constructed to mitigate adverse effects of a wireless channel, the equalizer comprising;

a delay line, coupled to an input signal and comprising a delay circuit coupled to an output combiner, the delay line operable to provide an interim signal; and

a feed forward circuit coupled to the delay line and operable to provide a feed forward signal that comprises a hard decision scaled according to a scaling factor corresponding to an estimate of channel parameters,

wherein the output combiner is operable to combine the feed forward signal and the interim signal to provide an output signal that is delayed relative to the input signal and compensated for an adverse effect of the wireless channel on the input signal.

2. The equalizer of claim 1 wherein the feed forward circuit further comprises a circuit coupled to the delay line and operable to provide the hard decision corresponding to a polarity of a signal at an input to the delay circuit and a scaling circuit operable to associate the polarity with the scaling factor to provide the feed forward signal and the output combiner is a summer that provides a linear combination of the feed forward signal and the interim signal as the output signal.

3. The equalizer of claim 1 further comprising a feedback circuit coupled to the delay line and operable to provide a feedback signal that is scaled according to an other scaling factor corresponding to the estimate of the channel parameters and wherein the delay line further comprises an input combiner operable to combine the feedback signal and the input signal to provide a signal at an input to the delay circuit.

4. The equalizer of claim 3 wherein the feedback circuit further comprises a circuit coupled to the delay line and operable to provide an other hard decision corresponding to a polarity of a signal at an output of the delay circuit and an other scaling circuit operable to associate the polarity with the other scaling factor to provide the feedback signal.

5. The equalizer of claim 3 wherein:

the delay line further comprises series coupled delay circuits;

the feed forward circuit further comprises N_f feed forward circuits each coupled to an input of any one of the series coupled delay circuits, the N_f feed forward circuits operable to provide N_f feed forward signals;

the output combiner is further operable to combine the N_f feed forward signals and the interim signal to provide the output signal;

the feedback circuit further comprises N_b feed back circuits each coupled to an output of the any one of the series coupled delay circuits, the N_b feedback circuits operable to provide N_b feedback signals; and

the input combiner is operable to combine the N_b feedback signals and the input signal to provide a signal at a first input of the series coupled delay circuits.

6. The equalizer of claim 5 wherein each of the N_f feed forward circuits further comprises a corresponding circuit coupled to the delay line and operable to provide a corresponding hard decision according to a polarity of a signal at the input and a corresponding scaling circuit operable to associate the polarity with the scaling factor to provide a corresponding one of the N_f feed forward signals and the output combiner is a summer that provides a linear combination of the N_f feed forward signals and the interim signal as the output signal.

7. The equalizer of claim 5 wherein each of the N_b feedback circuits further comprises a circuit coupled to the delay line and operable to provide an other hard decision corresponding to a polarity of a signal at the output and an other scaling circuit operable to associate the polarity with the other scaling factor to provide a corresponding one of the N_b feedback signals and the input combiner is an other summer that provides a linear combination of the N_b feedback signals and the input signal to provide the signal at the first input of the series coupled delay circuits.

8. The equalizer of claim 5 wherein the series coupled delay circuits comprises a number of series coupled delay circuits, where the number is equal to or greater than a larger one of N_f and N_b.

9. The equalizer of claim 5 wherein N_b is equal to or larger than N_f.

10. The equalizer of claim 3 wherein

the delay line further comprises series coupled delay circuits; and

the feed forward circuit comprises a feed forward look up table that is addressed according to a combination of feed forward hard decisions, each feed forward hard decision

corresponding to a polarity of an input signal at a different one of the series coupled delay circuits, the feed forward look up table operable to provide a unique linear combination of feed forward scaling factors as the feed forward signal for each unique one of the combination of feed forward hard decisions, the feed forward scaling factors corresponding to the estimate of the channel parameters.

11. The equalizer of claim 10 wherein the feedback circuit further comprises a feedback lookup table that is addressed according to a combination of feedback hard decisions, each feedback hard decision corresponding to a polarity of an output signal at an other different one of the series coupled delay circuits, the feedback lookup table operable to provide a unique linear combination of feedback scaling factors as the feedback signal for each unique one of the combination of feedback hard decisions, the feedback scaling factors corresponding to the estimate of the channel parameters.

12. The equalizer of claim 1 wherein the input signal corresponds to a Bipolar Phase Shift Keyed signal.

13. The equalizer of claim 1 arranged and constructed for use in a wireless receiver.

14. The equalizer of claim 1 implemented in an integrated circuit.

15. A method of equalizing in a receiver to mitigate adverse effects on a received signal caused by a wireless channel, the method comprising;

delaying a signal corresponding to an input signal with a delay function to provide an interim signal;

providing a feed forward signal that corresponds to the signal and comprises a hard decision scaled according to a feed forward scaling factor that corresponds to an estimate of channel parameters, and

combining the feed forward signal and the interim signal to provide an output signal that is delayed relative to the input signal and compensated for an adverse effect of the wireless channel on the input signal.

16. The method of claim 15 wherein the providing the feed forward signal further comprises providing the hard decision corresponding to a polarity of a signal at an input to the delay function and associating the polarity with the feed forward scaling factor to provide the feed

forward signal and the combining further comprises subtracting the feed forward signal from the interim signal to provide the output signal.

17. The method of claim 15 further comprising providing a feedback signal that is scaled according to a feedback scaling factor corresponding to the estimate of the channel parameters and combining the feedback signal and the input signal to provide the signal corresponding to the input signal at the input to the delay function.

18. The method of claim 17 wherein the providing the feedback signal further comprises providing an other hard decision corresponding to a polarity of a signal at an output of the delay function and associating the polarity with the feedback scaling factor to provide the feedback signal.

19. The method of claim 17 wherein:

the delaying the signal corresponding to the input signal further comprises delaying the signal with series coupled delay functions;

the providing the feed forward signal further comprises providing N_f feed forward signals each dependent on a corresponding hard decision and a corresponding feed forward scaling factor, the corresponding hard decision reflecting a polarity of a signal at an input of any one of the series coupled delay functions, the corresponding feed forward scaling factor associated with the polarity;

the combining the feed forward signal further comprises combining the N_f feed forward signals and the interim signal to provide the output signal;

the providing the feedback signal further comprises providing N_b feed back signals each dependent on a corresponding other hard decision and a corresponding feedback scaling factor, the corresponding other hard decision reflecting a polarity of a signal at an output of the any one of the series coupled delay functions and the corresponding feedback scaling factor associated with the polarity; and

the combining the feedback signal further comprises combining the N_b feedback signals and the input signal to provide a signal at a first input of the series coupled delay functions.

20. The method of claim 19 wherein the series coupled delay functions comprises a number of series coupled delay functions, where the number is equal to or greater than a larger one of N_f and N_b.

21. The method of claim 19 wherein N_b is equal to or larger than N_f.

22. The method of claim 16 wherein the providing the feed forward signal further comprises:

providing a plurality of unique linear combinations of feed forward scaling factors, the feed forward scaling factors corresponding to the estimate of the channel parameters; and

selecting one of the plurality of unique linear combinations of the feed forward scaling factors as the feed forward signal based on a combination of feed forward hard decisions, each feed forward hard decision corresponding to a polarity of an input signal at a different one of series coupled delay functions.

23. The method of claim 17 wherein the providing the feedback signal further comprises:

providing a plurality of unique linear combinations of feedback scaling factors, the feedback scaling factors corresponding to the estimate of the channel parameters;

selecting one of the plurality of unique linear combinations of feedback scaling factors as the feedback signal based on a combination of feedback hard decisions, each feedback hard decision corresponding to a polarity of an output signal at a different one of series coupled delay circuits.

24. The method of claim 15 wherein the input signal corresponds to a Bipolar Phase Shift Keyed signal.

25. The method of claim 15 practiced in an integrated circuit.

26. An equalizer arranged and constructed to mitigate adverse effects of a wireless channel on an M-ary signal, the equalizer comprising;

an input section coupled to an input signal corresponding to the M-ary signal and operable to provide a plurality of signals corresponding to a plurality of symbols;

a detector coupled to the plurality of signals for providing a hard decision indicative of one of the plurality of symbols;

a delay line comprising a delay circuit coupled to the hard decision and operable to provide a plurality of delay line hard decisions;

a feed forward section coupled to the delay line and operable to provide a plurality of feed forward signals, each comprising a feed forward scaling factor corresponding to a first one of the delay line hard decisions, the feed forward scaling factor corresponding to an estimate of

channel parameters, the plurality of feed forward signals corresponding to the plurality of signals; and

an output section with a plurality of combiners, each operable to a combine a corresponding one of the plurality of signals and a corresponding one of the plurality of feed forward signals to provide an output signal that is delayed relative to the input signal and compensated for an adverse effect of the wireless channel on the input signal.

27. The equalizer of claim 26 wherein the input section comprises a plurality of correlators, each operable to correlate the input signal with one of the plurality of symbols and provide one of a plurality of correlator signals that corresponds to one of the plurality of signals.

28. The equalizer of claim 26 wherein the delay line further comprises series coupled delay circuits; each successively delaying the hard decision to provide successive delay line hard decisions.

29. The equalizer of claim 26 wherein the feed forward section further comprises a plurality of feed forward scaling functions, each operable to select a first feed forward scaling factor corresponding to a first delay line hard decision and a second feed forward scaling factor corresponding to a second delay line hard decision, the first and second feed forward scaling factors associated with a corresponding one of the plurality of symbols and operable to combine the first and second feed forward scaling factors to provide a corresponding one of the plurality of feed forward signals.

30. The equalizer of claim 26 wherein the output section further comprises a delay line coupled to the plurality of signals and providing the plurality of signals delayed by the same amount as the delay line delays the hard decision.

31. The equalizer of claim 26 further comprising a feedback section coupled to the delay line and operable to provide a plurality of feedback signals, each comprising a feedback scaling factor corresponding to a second one of the plurality of delay line hard decisions, the feedback scaling factor corresponding to the estimate of channel parameters, the plurality of feedback signals corresponding to the plurality of signals; and

wherein the input section further comprises a plurality of input combiners, each operable to combine a corresponding one of a plurality of correlator signals and a corresponding one of the feedback signals to provide a corresponding one of the plurality of signals.

32. The equalizer of claim 31 wherein the feedback section further comprises a plurality of feedback functions, each operable to select a first feedback scaling factor corresponding to a first one of the plurality of delay line hard decisions and a second feedback scaling factor corresponding to a second one of the plurality of delay line hard decisions, the first and the second feedback scaling factors associated with a corresponding one of the plurality of symbols and each further operable to combine the first and second feedback scaling factors to provide a corresponding one of the plurality of feedback signals.

33. The equalizer of claim 31 wherein the feedback section further comprises a plurality of feedback look up tables, each operable to select a linear combination of feedback scaling factors corresponding to the plurality of the delay line hard decisions, the linear combination of feedback scaling factors associated with a corresponding one of the plurality of symbols and each further operable to provide the linear combination of feedback scaling factors as a corresponding one of the plurality of feedback signals.

34. The equalizer of claim 26 wherein the feed forward section further comprises a plurality of feed forward look up tables, each operable to select a linear combination of feed forward scaling factors corresponding to the plurality of delay line hard decisions, the linear combination of feed forward scaling factors associated with a corresponding one of the plurality of symbols and each further operable to provide the linear combination of feed forward scaling factors as a corresponding one of the plurality of feed forward signals.

35. The equalizer of claim 26 wherein the input signal corresponds to one of an M-ary signal and an M-ary Binary orthogonal keying signal.